

REMARKS

As set forth below, Applicant submits that the claimed invention is allowable over the cited reference because the Examiner fails to provide correspondence to aspects of the claimed invention directed to a parallel memory element.

The final Office Action dated September 18, 2007 indicated that claims 1-10 stand rejected under 35 U.S.C. 102(e) over Kanazashi (U.S. Patent No. 7,148,826).

Applicant respectfully traverses the Section 102(e) rejection of claims 1-10 because the cited portions of the Kanazashi reference do not correspond to the claimed invention which includes, for example, aspects directed to a parallel memory element coupled to a serial memory element. Kanazashi's Figure 5 discloses a shift register 14 (which the Examiner asserts as corresponding to Applicant's serial memory element); however, the Examiner fails to identify any part of Kanazashi as corresponding to Applicant's parallel memory element. Kanazashi teaches that the input data is supplied to the shift register 14 through the input buffer 10 in the order of the input data and that the input data is sequentially shifted through the columns (N3-N1') of the shift register 14. *See, e.g.*, Figure 5; Col. 2:61-64 and Col. 4:30-44. The input data stored in the columns (N3-N1') of the shift register 14 is then outputted to the data bus (A3, A2, A1, and A0). *See, e.g.*, Col. 4:53-67. Thus, the cited portions of Kanazashi do not teach that there is a parallel memory element coupled to the shift register 14. Accordingly, the Section 102(e) rejection of claims 1-10 is improper and Applicant requests that it be withdrawn.

In the event that the Examiner is asserting that Kanazashi's shift register 14 corresponds to both Applicant's serial memory element and parallel memory element, Applicant submits that such an assertion is inconsistent with the claimed invention when viewed as a whole. More specifically, the claimed invention includes aspects directed to the serial memory element having at least one more memory location than the parallel memory element. Asserting that Kanazashi's shift register 14 corresponds to both the serial memory element and the parallel memory element would mean that the memory elements taught by Kanazashi would have the same number of memory locations. Thus, the cited portions of Kanazashi would not correspond to the claimed invention.

Therefore, it would be improper for the Examiner to assert that Kanazashi's shift register 14 corresponds to both Applicant's serial memory element and Applicant's parallel memory element.

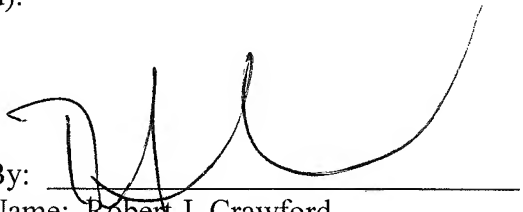
Applicant further traverses the Section 102(e) rejection of claims 3 and 5 because the cited portions of the Kanazashi reference do not correspond to aspects of the claimed invention directed to exchanging data between serial and parallel memory elements residing in different clock domains. As discussed above, the cited portions of Kanazashi do not teach or suggest a parallel memory element as claimed. Moreover, the cited portions of Kanazashi teach that input data is supplied to shift register 14 following internal clock CLK1 (*see, e.g.*, Figure 5 and 6A; Col. 4:40-43), but there is no mention of Kanazashi's external clock (cited by the Examiner) being used for reading the input data from a parallel memory element. Thus, the cited portions of Kanazashi do not teach transferring data between serial and parallel memory elements that reside in different clock domains as in the claimed invention. Accordingly, the Section 102(e) rejection of claims 3 and 5 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, David Cordeiro, of NXP Corporation at (408) 474-9061 (or the undersigned).

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